



PSMN1R4-40YLD

N-channel 40 V 1.4 m Ω logic level MOSFET in LPAK56 using NextPower-S3 technology

26 August 2014

Product data sheet

1. General description

Logic level gate drive N-channel enhancement mode MOSFET in 175 °C LPAK56 package using advanced TrenchMOS Superjunction technology. This product has been designed and qualified for high performance power switching applications.

2. Features and benefits

- NextPower-S3 technology delivers 'superfast switching with soft recovery'
- Low Q_{RR} , Q_G and Q_{GD} for high system efficiency and low EMI designs
- Schottky-Plus body-diode, gives soft switching without the associated high I_{DSS} leakage
- Optimised for 4.5 V gate drive utilising NextPower-S3 Superjunction technology
- High reliability LPAK (Power-SO8) package, copper-clip, solder die attach and qualified to 175 °C
- Exposed leads can be wave soldered, visual solder joint inspection and high quality solder joints
- Low parasitic inductance and resistance

3. Applications

- Synchronous rectification
- DC-to-DC converters
- High performance & high efficiency server power supply
- Motor control
- Power OR-ing

4. Quick reference data

Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|----------------------------------|---|-----|------|-----|------------|
| V_{DS} | drain-source voltage | $25\text{ °C} \leq T_j \leq 175\text{ °C}$ | - | - | 40 | V |
| I_D | drain current | $T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; Fig. 2 | [1] | - | 100 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C}$; Fig. 1 | - | - | 238 | W |
| T_j | junction temperature | | -55 | - | 175 | °C |
| Static characteristics | | | | | | |
| R_{DSon} | drain-source on-state resistance | $V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 10 | - | 1.12 | 1.4 | m Ω |



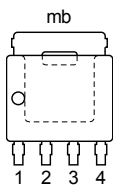
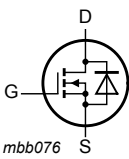
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| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|-------------------|--|-----|------|------|------|
| | | $V_{GS} = 4.5\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ }^\circ\text{C};$ Fig. 10 | - | 1.38 | 1.85 | mΩ |
| Dynamic characteristics | | | | | | |
| Q_{GD} | gate-drain charge | $V_{GS} = 4.5\text{ V}; I_D = 25\text{ A}; V_{DS} = 20\text{ V};$ Fig. 12; Fig. 13 | - | 13 | - | nC |
| $Q_{G(\text{tot})}$ | total gate charge | $V_{GS} = 4.5\text{ V}; I_D = 25\text{ A}; V_{DS} = 20\text{ V};$ Fig. 12; Fig. 13 | - | 45 | - | nC |

[1] Continuous current is limited by package.

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-----------------------------------|--|--|
| 1 | S | source |  <p>LFAK56; Power-SO8 (SOT669)</p> |  <p>mbb076</p> |
| 2 | S | source | | |
| 3 | S | source | | |
| 4 | G | gate | | |
| mb | D | mounting base; connected to drain | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|---------------|-------------------|---|---------|
| | Name | Description | Version |
| PSMN1R4-40YLD | LFAK56; Power-SO8 | Plastic single-ended surface-mounted package (LFAK56; Power-SO8); 4 leads | SOT669 |

7. Marking

Table 4. Marking codes

| Type number | Marking code |
|---------------|--------------|
| PSMN1R4-40YLD | 1D440L |

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|-----------------------------|--|--|-----|-----|------|------|
| V _{DS} | drain-source voltage | 25 °C ≤ T _j ≤ 175 °C | | - | 40 | V |
| V _{DSM} | peak drain-source voltage | t _p ≤ 20 ns; f ≤ 500 kHz; E _{DS(AL)} ≤ 200 nJ; pulsed | | - | 45 | V |
| V _{DGR} | drain-gate voltage | 25 °C ≤ T _j ≤ 175 °C; R _{GS} = 20 kΩ | | - | 40 | V |
| V _{GS} | gate-source voltage | | | -20 | 20 | V |
| P _{tot} | total power dissipation | T _{mb} = 25 °C; Fig. 1 | | - | 238 | W |
| I _D | drain current | V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2 | [1] | - | 100 | A |
| | | V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2 | [1] | - | 100 | A |
| I _{DM} | peak drain current | pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3 | | - | 1201 | A |
| T _{stg} | storage temperature | | | -55 | 175 | °C |
| T _j | junction temperature | | | -55 | 175 | °C |
| T _{slid(M)} | peak soldering temperature | | | - | 260 | °C |
| V _{ESD} | electrostatic discharge voltage | HBM | | 2 | - | kV |
| Source-drain diode | | | | | | |
| I _S | source current | T _{mb} = 25 °C | [1] | - | 100 | A |
| I _{SM} | peak source current | pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C | | - | 1201 | A |
| Avalanche ruggedness | | | | | | |
| E _{DS(AL)S} | non-repetitive drain-source avalanche energy | T _{j(initial)} = 25 °C; I _D = 74 A; R _{GS} = 50 Ω; unclamped; t _p = 0.23 ms; V _{GS} = 10 V; V _{sup} ≤ 40 V | [2] | - | 446 | mJ |
| | | V _{GS} = 10 V; T _{j(initial)} = 25 °C; I _D = 25 A; V _{sup} ≤ 40 V; R _{GS} = 50 Ω; unclamped; t _p = 2.52 ms | [2] | - | 1641 | mJ |

[1] Continuous current is limited by package.

[2] Protected by 100% test

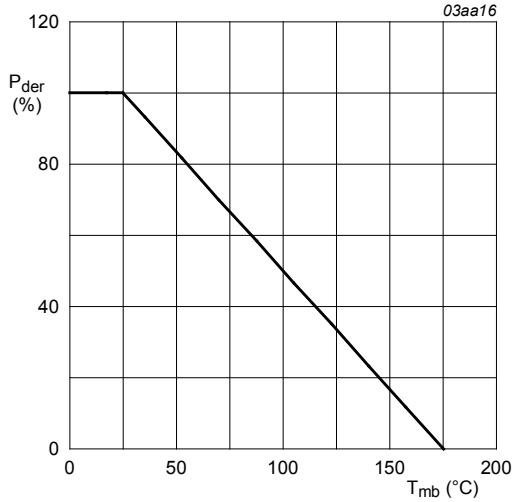
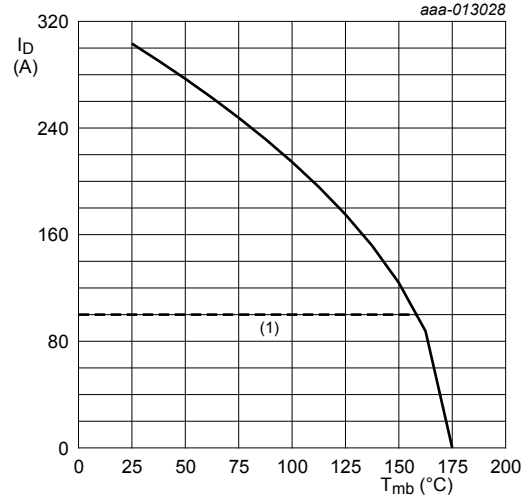


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$



(1) Capped at 100A due to package

Fig. 2. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 5V$$

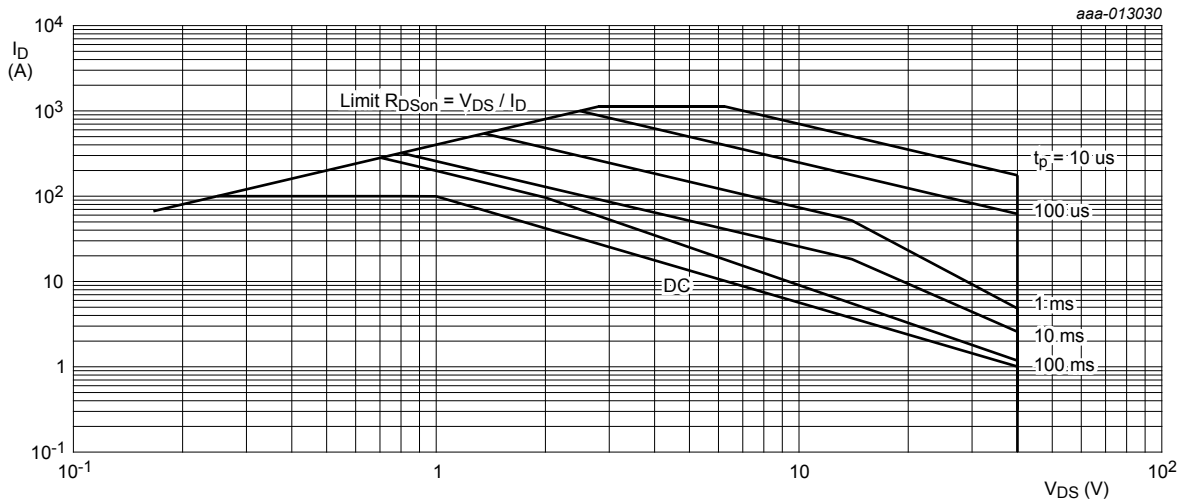


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$$T_{mb} = 25^\circ C; I_{DM} \text{ is a single pulse}$$

9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|---|------------|-----|------|------|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Fig. 4 | - | 0.56 | 0.63 | K/W |

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| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------|---|------------------------|-----|-----|-----|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | Fig. 5 | - | 50 | - | K/W |
| | | Fig. 6 | - | 125 | - | K/W |

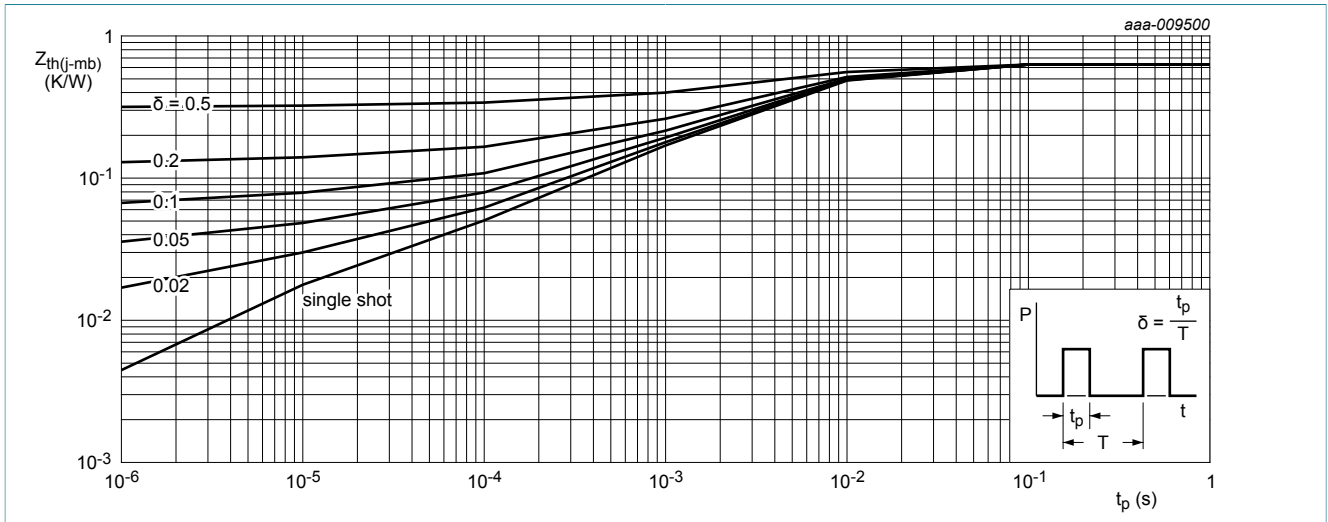


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

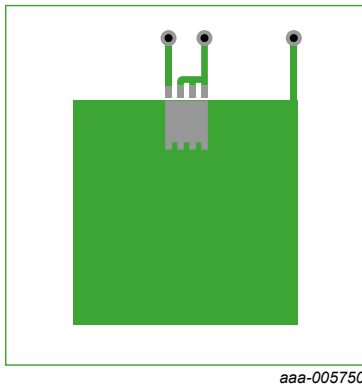


Fig. 5. PCB layout for thermal resistance junction to ambient 1" square pad; FR4 Board; 2oz copper

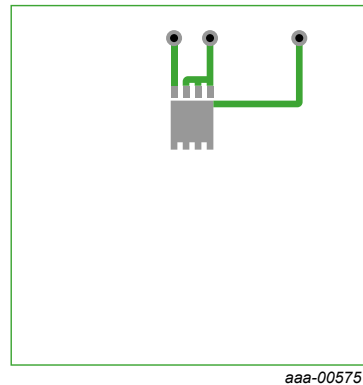


Fig. 6. PCB layout for thermal resistance junction to ambient minimum footprint; FR4 Board; 2oz copper

10. Characteristics

Table 7. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|--------------------------------|--|------|-----|-----|------|
| Static characteristics | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$ | 40 | - | - | V |
| | | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$ | 36 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$ | 1.05 | 1.7 | 2.2 | V |

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| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|--|---|-----|------|------|------|
| $\Delta V_{GS(th)}/\Delta T$ | gate-source threshold voltage variation with temperature | $25\text{ °C} \leq T_j \leq 150\text{ °C}$ | - | -4.8 | - | mV/K |
| I_{DSS} | drain leakage current | $V_{DS} = 32\text{ V}; V_{GS} = 0\text{ V}; T_j = 25\text{ °C}$ | - | - | 1 | μA |
| | | $V_{DS} = 32\text{ V}; V_{GS} = 0\text{ V}; T_j = 125\text{ °C}$ | - | 12 | - | μA |
| I_{GSS} | gate leakage current | $V_{GS} = 16\text{ V}; V_{DS} = 0\text{ V}; T_j = 25\text{ °C}$ | - | - | 100 | nA |
| | | $V_{GS} = -16\text{ V}; V_{DS} = 0\text{ V}; T_j = 25\text{ °C}$ | - | - | 100 | nA |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C};$ Fig. 10 | - | 1.12 | 1.4 | mΩ |
| | | $V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 175\text{ °C};$ Fig. 11; Fig. 10 | - | - | 2.65 | mΩ |
| | | $V_{GS} = 4.5\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C};$ Fig. 10 | - | 1.38 | 1.85 | mΩ |
| | | $V_{GS} = 4.5\text{ V}; I_D = 25\text{ A}; T_j = 175\text{ °C};$ Fig. 11; Fig. 10 | - | - | 3.4 | mΩ |
| R_G | gate resistance | $f = 1\text{ MHz}$ | - | 1.1 | - | Ω |
| Dynamic characteristics | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D = 25\text{ A}; V_{DS} = 20\text{ V}; V_{GS} = 10\text{ V};$ Fig. 12; Fig. 13 | - | 96 | - | nC |
| | | $I_D = 25\text{ A}; V_{DS} = 20\text{ V}; V_{GS} = 4.5\text{ V};$ Fig. 12; Fig. 13 | - | 45 | - | nC |
| | | $I_D = 0\text{ A}; V_{DS} = 0\text{ V}; V_{GS} = 10\text{ V}$ | - | 85 | - | nC |
| Q_{GS} | gate-source charge | $I_D = 25\text{ A}; V_{DS} = 20\text{ V}; V_{GS} = 4.5\text{ V};$ Fig. 12; Fig. 13 | - | 15 | - | nC |
| $Q_{GS(th)}$ | pre-threshold gate-source charge | | - | 9 | - | nC |
| $Q_{GS(th-pl)}$ | post-threshold gate-source charge | | - | 6 | - | nC |
| Q_{GD} | gate-drain charge | | - | 13 | - | nC |
| $V_{GS(pl)}$ | gate-source plateau voltage | $I_D = 25\text{ A}; V_{DS} = 20\text{ V};$ Fig. 12; Fig. 13 | - | 2.7 | - | V |
| C_{iss} | input capacitance | $V_{DS} = 20\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ °C};$ Fig. 14 | - | 6661 | - | pF |
| C_{oss} | output capacitance | | - | 1543 | - | pF |
| C_{rss} | reverse transfer capacitance | | - | 299 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS} = 20\text{ V}; R_L = 0.8\text{ Ω}; V_{GS} = 4.5\text{ V};$ $R_{G(ext)} = 5\text{ Ω}$ | - | 39 | - | ns |
| t_r | rise time | | - | 49 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 47 | - | ns |
| t_f | fall time | | - | 30 | - | ns |

N-channel 40 V 1.4 mΩ logic level MOSFET in LFPAK56 using NextPower-S3 technology

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------------|----------------------------|---|-----|------|-----|------|
| Q_{oss} | output charge | $V_{GS} = 0\text{ V}; V_{DS} = 20\text{ V}; f = 1\text{ MHz}; T_j = 25\text{ }^\circ\text{C}$ | - | 50 | - | nC |
| Source-drain diode | | | | | | |
| V_{SD} | source-drain voltage | $I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 15}$ | - | 0.78 | 1.2 | V |
| t_{rr} | reverse recovery time | $I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 20\text{ V}; \text{Fig. 16}$ | - | 47 | - | ns |
| Q_r | recovered charge | [1] | - | 61 | - | nC |
| t_a | reverse recovery rise time | $I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 20\text{ V}; \text{Fig. 16}$ | - | 25.4 | - | ns |
| t_b | reverse recovery fall time | | - | 21.7 | - | ns |

[1] includes capacitive recovery

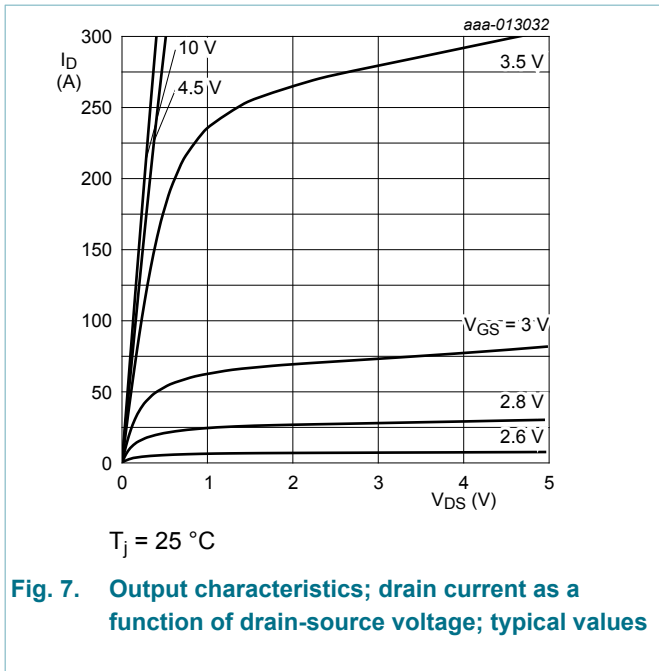


Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values

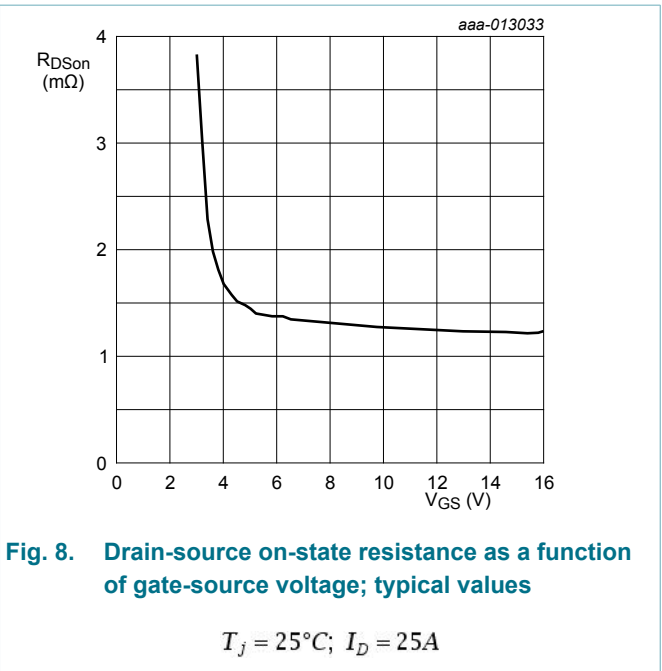


Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25\text{ }^\circ\text{C}; I_D = 25\text{ A}$

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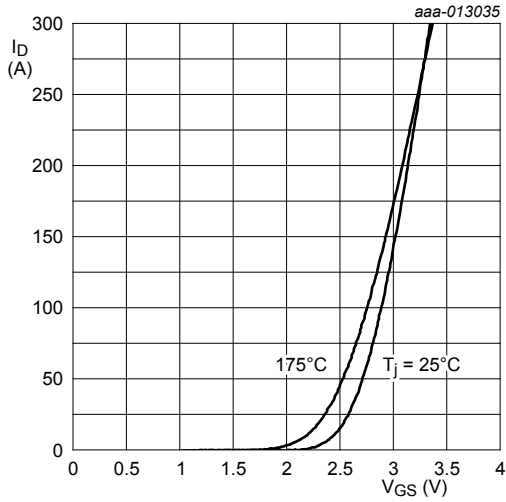


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$$V_{DS} = 10V$$

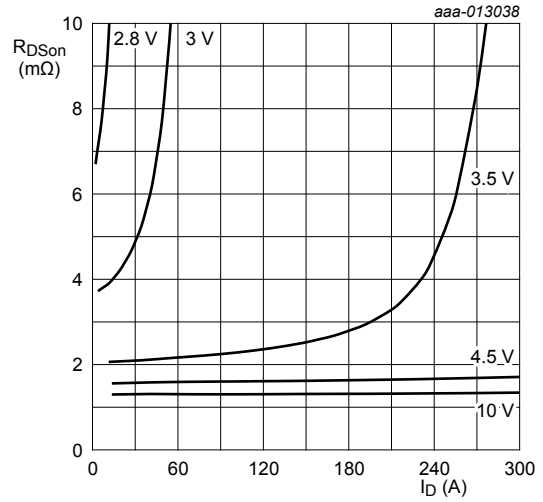


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25\text{ }^\circ\text{C}$$

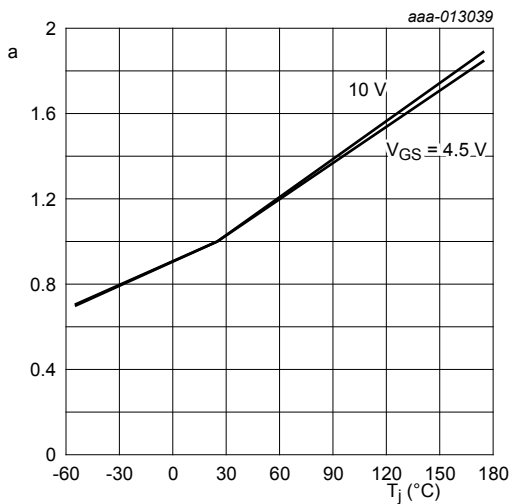


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

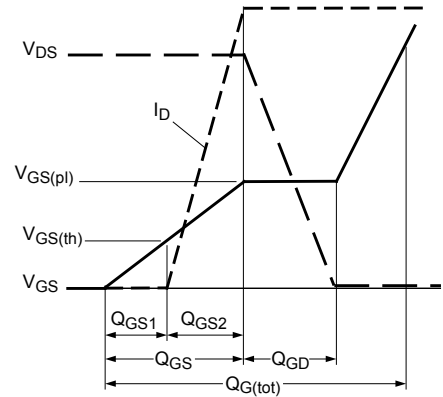


Fig. 12. Gate charge waveform definitions

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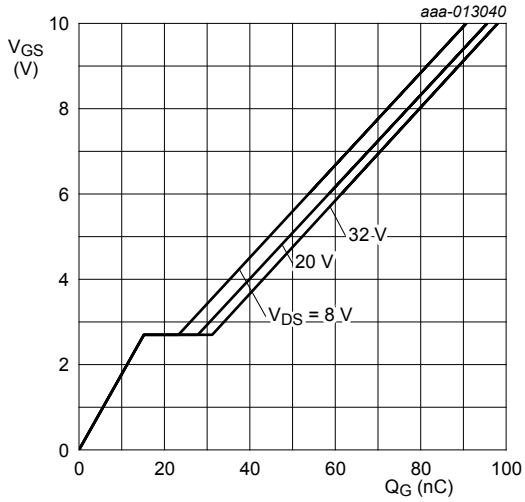


Fig. 13. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^\circ\text{C}; I_D = 25\text{A}$$

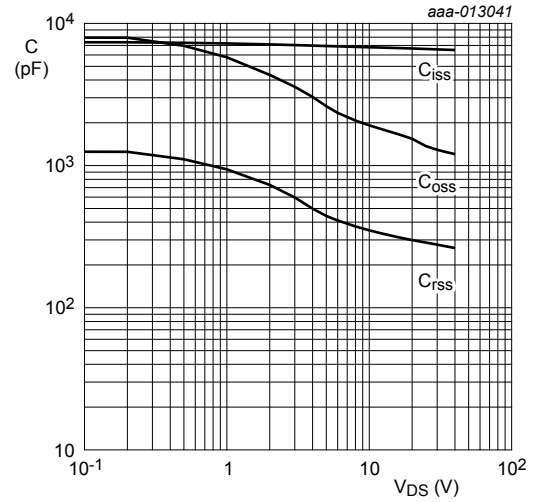


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0\text{V}; f = 1\text{MHz}$$

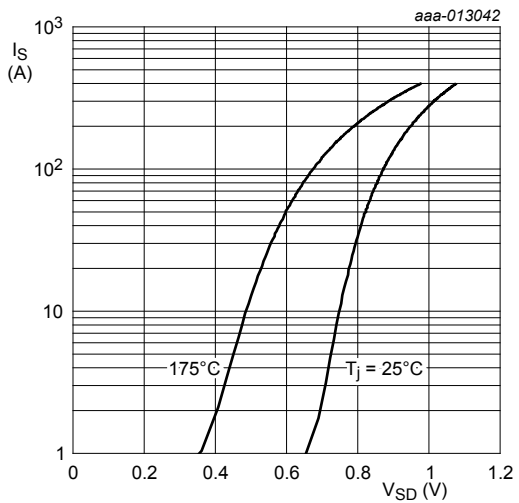


Fig. 15. Source current as a function of source-drain voltage; typical values

$$V_{GS} = 0\text{V}$$

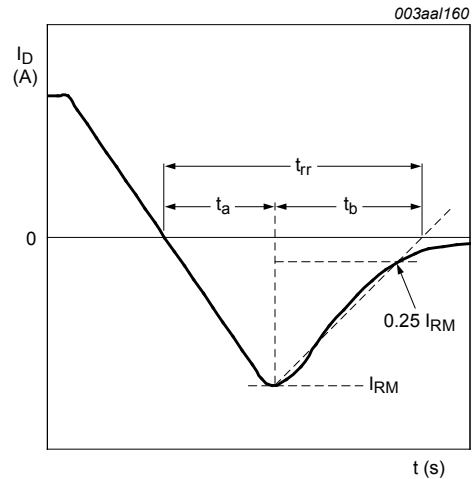


Fig. 16. Reverse recovery timing definition

11. Package outline

Plastic single-ended surface-mounted package (LPAK56; Power-SO8); 4 leads SOT669



Dimensions (mm are the original dimensions)

| Unit ⁽¹⁾ | A | A ₁ | A ₂ | A ₃ | b | b ₂ | b ₃ | b ₄ | c | c ₂ | D ⁽¹⁾ | D ₁ ⁽¹⁾ | E ⁽¹⁾ | E ₁ ⁽¹⁾ | e | H | L | L ₁ | L ₂ | w | y |
|---------------------|------|----------------|----------------|----------------|------|----------------|----------------|----------------|------|----------------|------------------|-------------------------------|------------------|-------------------------------|------|-----|------|----------------|----------------|------|-----|
| max | 1.20 | 0.15 | 1.10 | | 0.50 | 4.41 | 2.2 | 0.9 | 0.25 | 0.30 | 4.10 | 4.20 | 5.0 | 3.3 | | 6.2 | 0.85 | 1.3 | 1.3 | | |
| nom | | | | 0.25 | | | | | | | | | | | 1.27 | | | | | 0.25 | 0.1 |
| min | 1.01 | 0.00 | 0.95 | | 0.35 | 3.62 | 2.0 | 0.7 | 0.19 | 0.24 | 3.80 | | 4.8 | 3.1 | | 5.8 | 0.40 | 0.8 | 0.8 | | |

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

sot669_po

| Outline version | References | | | | European projection | Issue date |
|-----------------|------------|--------|-------|--|---------------------|------------------------|
| | IEC | JEDEC | JEITA | | | |
| SOT669 | | MO-235 | | | | -11-03-25- 13-02-27 |

Fig. 17. Package outline LPAK56; Power-SO8 (SOT669)

12. Legal information

12.1 Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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